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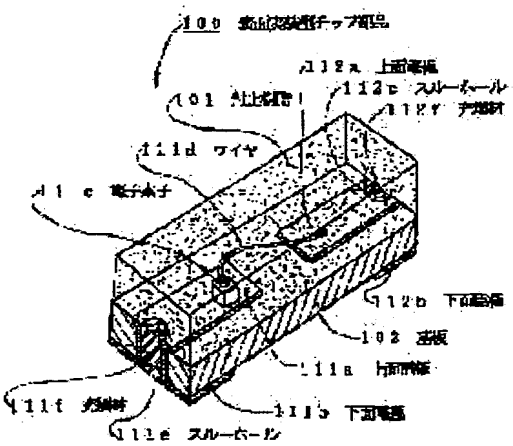
(54) SURFACE MOUNT CHIPS AND THEIR MANUFACTURE

(57)Abstract:
PROBLEM TO BE SOLVED: To obtain a highly reliable surface mount chip which can be reduced in size and thickness, by filling up through holes with a conductive member.

SOLUTION: A chip 100 is constituted of a substrate 102 made of a glass epoxy material, etc., and a sealing resin 101 molded on the upper surface of the substrate 102. Upper-surface electrodes 111a and 112a and lower-surface electrodes 111b and 112b are provided on the substrate 102, and the electrodes 111a and 112a are respectively connected to the electrodes 111b and 112n through through holes 111e and 112e. The holes 111e and 112e are respectively filled up with fillers 111f and 112f by screen-printing a conductive material such as the conductive adhesive, solder, etc. Since the sizes of the sealing resin 101 and the substrate 102 can be made equal to each other, a very small surface mount chip can be obtained. In addition, the flow of the sealing resin in the through holes 111e and 112e can be prevented completely, because the holes 111e and 112e are filled up with the conductive material.



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* NOTICES *

CLAIMS

[Claim(s)]
[Claim 1] The surface mount mold chip characterized by to fill up with and constitute said through hole from a conductive member in the surface mount mold chip which arranged an electronic device on said top-face electrode of set substrates, such as a paper phenol or glass epoxy material which prepared two or more vertical side electrodes which have a through hole, connected this electronic device to said top-face electrode and the approaching electrode by wirebonding etc., carried out the mold of said electronic device by closure resin on said set substrate, and was constituted by carrying out cutting division.
[Claim 2] Said conductive member is electroconductive glue, anisotropy electric conduction adhesives, an anisotropy electric conduction sheet, solder, and a surface mount mold chip according to claim 1 characterized by any in a silver paste, or being one.
[Claim 3] The surface mount mold chip according to claim 1 characterized by carrying out the mold of the top-face electrode surface side connected with said through hole filled up with said conductive member by said closure resin.
[Claim 4] The surface mount mold chip according to claim 1 with which said through hole is characterized by being formed in the substrate end face of said surface mount mold chip.
[Claim 5] The surface mount mold chip according to claim 4 characterized by forming said through hole in the end side of a substrate more than a piece at least.
[Claim 6] An electronic device is arranged in said top-face electrode of set substrates, such as a paper phenol or glass epoxy material which prepared two or more vertical side electrodes which have a through hole. In the manufacture approach of the surface mount mold chip which connected this electronic device to said top-face electrode and the approaching electrode by wirebonding etc., carried out the mold of said electronic device by closure resin on said set substrate, and was constituted by carrying out cutting division The process which prepares two or more vertical side electrodes which have a through hole on said set substrate at a column row, The process which fills up said through hole with a conductive member, and the process which arranges said electronic device in said electrode, The process which connects said electronic device to the approaching electrode by wirebonding etc., The process which carries out the mold of said electronic device by closure resin on said set substrate, and the process which cuts the through hole train prepared in said column row in said substrate thickness direction with said closure resin by which mold was carried out, The manufacture approach of the surface mount mold chip characterized by for the process which cuts [direction / said / cutting] the periphery section of said vertical side electrode train in the thickness direction of said set substrate with closure resin in the direction of a right angle mostly dividing, and forming as a chip.
[Claim 7] The manufacture approach of the surface mount mold chip according to claim 6 characterized by carrying out the mold of the top-face electrode surface side connected with said through hole filled up with said conductive member by said closure resin.
[Claim 8] The manufacture approach of a surface mount mold chip according to claim 6 that said through hole is characterized by being formed in the substrate end face of said surface mount mold chip.
[Claim 9] The manufacture approach of the surface mount mold chip according to claim 8 characterized by forming said through hole in the end side of a substrate more than a piece at least.

[Translation done.]

* NOTICES *

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the electronic parts which carried out the resin mold of the electronic device. Furthermore, it is related with the configuration and the manufacture approach of the surface mount mold chip suitable for the surface mount of a printed circuit board in detail.
[0002]
[Description of the Prior Art] An electronic device is arranged in the top face of a substrate, and the electronic parts which carried out the mold of the top-face side of a substrate by closure resin including the electronic device are known well. Moreover, according to the miniaturization thin form-ized inclination of electronic equipment, the printed circuit board is asked for the electronic parts in which a surface mount is possible, i.e., a surface mount mold chip, and still much more miniaturization thin form-ization is expected. The surface mount mold chip (following chip) has a form near a rectangular parallelepiped block, and an electrode terminal is in the side face near the base or base, it is arranged by the circuit pattern on a printed circuit board, and has the composition that the electrode terminal which touched the circuit pattern is easily connectable with electroconductive glue, in many cases. Below, the configuration and the manufacture approach of a chip of the conventional example are explained.
[0003] Drawing 12 is the perspective view of the chip of the conventional example (1). Drawing 13 is the perspective view of the chip of the conventional example (2). Drawing 14 (a), (b) - drawing 17 (a), and (b) are the explanatory views of the main production processes 1-4 of the conventional example (1), it is the perspective view of a set substrate and this drawing (b) is [this drawing (a)] the fragmentary sectional view ****. Drawing 18 (a), (b) - drawing 21 (a), and (b) are the explanatory views of the main production processes 1-4 of the conventional example (2), it is the perspective view of a set substrate and this drawing (b) is [this drawing (a)] the fragmentary sectional view ****. Drawing 22 - drawing 24 are the through hole section detail explanatory views of the set substrate cross section of the conventional example.
[0004] In drawing 12 , a chip 200 is constituted from closure resin 201 by which mold was carried out by the top face of the substrates 202, such as paper phenol material and glass epoxy material, and a substrate 202. The top-face electrodes 211a and 212a and the inferior-surface-of-tongue electrodes 211b and 212b with which copper foil was formed by etching etc. are prepared in a substrate 202, and the top-face electrodes 211a and 212a and the inferior-surface-of-tongue electrodes 211b and 212b are through hole 211e, respectively. 212e connects. And said through holes 211e and 212e are on the through hole train cut line which put in a row the through hole mentioned later, it is mostly cut in the thickness direction of a substrate 202 along the core, and the cross section is mostly formed in the hemicycle. For example, electronic device 211c which consists of luminescence or a photo detector is arranged in top-face electrode 211a by die bonding etc., and the pad of electronic device 211c is connected to top-face electrode 212a which approaches by bonding wire 211d. ** and closure resin 201 are detached and formed from through holes 211e and 212e, in order to avoid that avoiding and the resin which flowed in carry out cure postcure of resin flowing into through holes 211e and 212e at the time of mold, cover the front face of the inferior-surface-of-tongue electrodes 211b and 212b, and defective continuity arises between printed circuit boards. Therefore, the substrate 202 needed to be made larger than the magnitude of closure resin 201, and made the miniaturization of a chip difficult.
[0005] If a chip 250 avoids duplication and only difference with drawing 12 is explained in drawing 13 , the slot through hole sides 281a and 282a formed from the slot through hole mentioned later will be established in the both ends of a substrate 252. The arrangement relation between the top-face electrodes 251a and 252a, the inferior-surface-of-tongue electrodes 251b and 252b, and the slot through hole sides 281a and 282a is the same as that of drawing 12 . In order, as for closure resin 251, to avoid that resin flows in the through hole sides 281a and 282a at the time of mold like drawing 12 also in this case, it is detached and prepared from the through hole sides 281a and 282a. Therefore, the substrate 252 needed to be made larger than the magnitude of closure resin 251, and made the miniaturization of a chip difficult similarly.
[0006] Next, the manufacture approach of the conventional example (1) is explained. In the process 1 of drawing 14 (a) and this drawing (b), the through hole of the set substrate 205 is arranged on the constant spacing ****** through hole train cut lines Y1 and Y2 decided on a design, and —YN. Similarly, said vertical side electrode is arranged in the constant spacing ****** chip cut lines X1 and X2 decided on a design, and —XN. It connects by through holes 211e, 212e, and 213e and —, and the top-face electrodes 211a and 212a, 213a— and they, the inferior-surface-of-tongue electrodes 211b, 212b, and 213b that correspond, respectively, and — (drawing abbreviation) are arranged by the column in X1 and X2 line. A vertical side electrode train is arranged by the set substrate 205 like the following.
[0007] In the process 2 of drawing 15 (a) and this drawing (b), electronic devices 211c and 212c and — are arranged in the top-face electrodes 211a and 212a and — by die bonding etc., respectively, and a pad is connected to approaching top-face electrode 213a of electronic devices 211c and 212c and —, and — by wirebonding etc. with Wires 211d and 212d.
[0008] In the process 3 of drawing 16 (a) and this drawing (b), adhesion loading is carried out so that the metal mold 203 which has window frames 203a, 203b, and 203c and — on the top face of the set substrate 205 may cover said through hole train.
[0009] In the process 4 of drawing 17 (a) and this drawing (b), the cure of the set closure resin (for example, epoxy system resin) 204a, 204b, and 204c is filled up with and carried out into metal mold 203. After cure hardening, if metal mold 203 is removed and dicing, a

slicing machine, etc. cut the set substrate 205 in the thickness direction according to the through hole train cut lines Y1 and Y2, —YN and the chip cut lines X1 and X2, —XN, the chip 200 of drawing 1212 can be obtained.
[0010] Next, duplication for the conventional example (1) is avoided and the production process which shows the conventional example (2) is explained. In the process 1 of drawing 18 (a) and this drawing (b), the slot through holes 281 and 282 of the set substrate 255 and — are arranged at constant spacing detached building ****** decided on a design. Similarly, the top-face electrodes 261a and 262a and — are arranged in the constant spacing ****** chip cut lines X1 and X2 decided on a design, and —XN, it connects by the slot through holes 281 and 282 and —, and said top-face electrode and inferior-surface-of-tongue electrode 261b, and 262b— are arranged by the column in X1 and X2 line. A vertical side electrode train is arranged by the set substrate 255 like the following.
[0011] In the process 2 of drawing 19 (a) and this drawing (b), electronic device 261c and 262c— is arranged in the top-face electrodes 261a and 263a and — by die bonding etc., respectively, and a pad is connected to approaching top-face electrode 262a of electronic devices 261c and 262c and —, and — by wirebonding etc. with Wires 261d and 262d.
[0012] In the process 3 of drawing 20 (a) and this drawing (b), adhesion loading is carried out so that the metal mold 253 which has window frames 253a and 253b and — on the top face of the set substrate 255 may cover the slot through holes 281 and 282.
[0013] In the process 4 of drawing 21 (a) and this drawing (b), the cure of the set closure resin (for example, epoxy system resin) 254a and 254b is filled up with and carried out into metal mold 253. If metal mold 253 is removed after cure hardening and dicing, a slicing machine, etc. cut the set substrate 255 in the thickness direction according to the chip cut lines X1 and X2 and —XN, the slot through holes 281 and 282 can form the slot through hole sides 281a and 282a of a chip, and can obtain the chip 250 of drawing 13 .
[0014] Drawing 22 shows the through hole section detail explanatory view of the cross section of the set substrate 205 of the conventional example (1), and since metal mold 203 has closed through holes 211e and 212e and —, closure resin 204a and 204b and the influx of — are not produced. Since the same is said of the slot through hole of the set substrate 255 of the conventional example (2), explanation is omitted.
[0015] Drawing 23 is another conventional example, and since the through hole 291 is closed by the resist 290, the influx of closure resin 293 is not produced.
[0016] Drawing 24 is another conventional example further, and since the through hole 291 is closed by the same copper foil as an electrode, and the plating material 294, the influx of closure resin 293 is not produced.
[0017]
[Problem(s) to be Solved by the Invention] However, there were the following problems in the conventional chip. As the conventional example (1) shows to drawing 12 , closure resin 201 is through hole 211e. In order to avoid flowing into 212e at the time of mold, or in order to avoid that the resin which flowed in carries out cure postcure, and the defective continuity between an inferior-surface-of-tongue electrode and a printed circuit board arises, it is necessary to separate through holes 211e and 212e from closure resin 201. Consequently, the substrate 202 is greatly formed from the magnitude of closure resin 201. For this reason, difficult [the miniaturization of a chip], only the part with a large substrate required the cost of materials, and cost/performance has not been improved.
[0018] Moreover, also in the conventional example (2), the slot through holes 281 and 282 need to separate from closure resin 251 for the same reason as the case of the above-mentioned conventional example (1). Consequently, the substrate 252 is greatly formed from the magnitude of closure resin 251. Although the through hole became a slot and the production process was simplified a little, like the above-mentioned conventional example (1) as a technical problem, difficult [the miniaturization of a chip], only the part with a large substrate required the cost of materials, and cost/performance has not been improved.
[0019] Moreover, in the fragmentary sectional view of the through hole section showing another conventional example, and drawing 23 , since there was a lid of a resist 290, although an influx to the through hole 291 of closure resin 293 was not produced, the air bubbles 292 produced in the inferior-surface-of-tongue part of a resist 290 could not fall out, and a top-face electrode and an inferior-surface-of-tongue electrode could not be connected by plating, but there was a problem that defective continuity occurred.
[0020] moreover, in the fragmentary sectional view of the through hole section showing another conventional example, and drawing 24 Since there is a lid of the same copper foil as an electrode or the plating material 294, although an influx to the through hole 291 of closure resin 293 is not produced The air bubbles 292 produced in the inferior-surface-of-tongue parts of the same copper foil as an electrode or the plating material 294 did not fall out, but like the above-mentioned conventional example, a top-face electrode and an inferior-surface-of-tongue electrode could not be connected by plating, but there was a problem that defective continuity occurred.
[0021] The purpose of this invention removes the above-mentioned fault, and the formation of a small thin form is possible for it, and it proposes a reliable surface mount mold chip and its manufacture approach.
[0022]
[Means for Solving the Problem] In order to attain the above-mentioned purpose, the surface mount mold chip in this invention arranges an electronic device on said top-face electrode of set substrates, such as a paper phenol or glass epoxy material which prepared two or more vertical side electrodes which have a through hole. In the surface mount mold chip which connected this electronic device to said top-face electrode and the approaching electrode by wirebonding etc., carried out the mold of said electronic device by closure resin on said set substrate, and was constituted by carrying out cutting division It is characterized by filling up with and constituting said through hole from a conductive member.
[0023] Moreover, it is characterized by said conductive member being any in electroconductive glue, anisotropy adhesives, an anisotropy electric conduction sheet, solder, and a silver paste, or one.
[0024] Moreover, it is characterized by carrying out the mold of the top-face electrode surface side connected with said through hole filled up with said conductive member by said closure resin.
[0025] Moreover, said through hole is characterized by being formed in the substrate end face of said surface mount mold chip.
[0026] Moreover, it is characterized by forming said through hole in the end side of a substrate more than a piece at least.
[0027] Moreover, the manufacture approach of the surface mount mold chip in this invention arranges an electronic device in said top-face electrode of set substrates, such as a paper phenol or glass epoxy material which prepared two or more vertical side electrodes which have a through hole. In the manufacture approach of the surface mount mold chip which connected this electronic device to said top-face electrode and the approaching electrode by wirebonding etc., carried out the mold of said electronic device by closure resin on said set substrate, and was constituted by carrying out cutting division The process which prepares two or more vertical side electrodes which have a through hole on said set substrate at a column row, The process which fills up said through hole with a

conductive member, and the process which arranges said electronic device in said electrode, The process which connects said electronic device to the approaching electrode by wirebonding etc., The process which carries out the mold of said electronic device by closure resin on said set substrate, and the process which cuts the through hole train prepared in said column row in said substrate thickness direction with said closure resin by which mold was carried out, It is characterized by for the process which cuts [direction / said / cutting] the periphery section of said vertical side electrode train in the thickness direction of said set substrate with closure resin in the direction of a right angle mostly dividing, and forming as a chip.

[0028] Moreover, the manufacture approach of this invention is characterized by carrying out the mold of the top-face electrode surface side connected with said through hole filled up with said conductive member by said closure resin.

[0029] Moreover, the manufacture approach of this invention is characterized by forming said through hole in the substrate end face of said surface mount mold chip.

[0030] Furthermore, the manufacture approach of this invention is characterized by forming said through hole in the end side of a substrate more than a piece at least.

[0031]

[Embodiment of the Invention] Below, the gestalt of operation of this invention is explained based on a drawing. Drawing 1 is the perspective view of the chip of this invention. Drawing 2 is the perspective view of other chips by this invention. Drawing 3 (a), (b) - drawing 6 (a), and (b) are the explanatory views of the main production processes 1-4 of the chip of this invention, this drawing (a) is a perspective view of a set substrate, and this drawing (b) is the sectional view. Drawing 7 (a), (b) - drawing 10 (a), and (b) are the explanatory views of the main production processes 1-4 of other chips by this invention, this drawing (a) is a perspective view of a set substrate, and this drawing (b) is the sectional view. Drawing 11 is the through hole section detail explanatory view of a set substrate cross section showing this invention.

[0032] In drawing 1 , the chip 100 of this invention is constituted from closure resin 101 by which mold was carried out by the top face of the substrates 102, such as glass epoxy material, and a substrate 102. The top-face electrodes 111a and 112a and the inferior-surface-of-tongue electrodes 111b and 112b with which copper foil was formed by etching etc. are prepared in a substrate 102, and the top-face electrodes 111a and 112a and the inferior-surface-of-tongue electrodes 111b and 112b are connected by through holes 111e and 112e, respectively. And through holes 111e and 112e are on the through hole train cut line mentioned later, it is mostly cut in the thickness direction of a substrate 102 along a core, and the cross section is mostly formed in the hemicycle. For example, electronic device 111c which consists of luminescence or a photo detector is arranged in top-face electrode 111a by die bonding, and the pad of electronic device 111c is connected to top-face electrode 112a which approaches by bonding wire 111d. Moreover, through holes 111e and 112e are filled up with conductive members, such as electroconductive glue or solder, by screen-stencil etc. as fillers 111f and 112f. In addition, as a conductive member, it can choose out of the inside of anisotropy electric conduction adhesives, an anisotropy electric conduction sheet, a silver paste, etc. suitably besides the aforementioned object.

[0033] In drawing 2 , if the chip 150 of this invention avoids duplication and only difference with drawing 1 is explained, the slot through hole sides 181a and 182a mentioned later will be established in the both ends of a substrate 152. The arrangement relation between the top-face electrodes 161a and 162a, the inferior-surface-of-tongue electrodes 161b and 162b, and the slot through hole sides 181a and 182a is the same as that of drawing 1 . In addition, screen-stencil etc. is filled up with conductive members, such as electric conduction adhesives or solder, as fillers 183a and 184a the slot through hole sides 181a and 182a.

[0034] Next, the manufacture approach of the chip 100 of this invention is explained. In the process 1 of drawing 3 (a) and this drawing (b), the through hole of the set substrate 105 is arranged on the constant spacing ****** through hole train cut lines Y1 and Y2 decided on a design, and —YN. Similarly, said vertical side electrode is arranged in the constant spacing ****** chip cut lines X1 and X2 decided on a design, and —XN. It connects by through holes 111e and 112e and —, and the top-face electrodes 111a, 112a, and 113a, — and they, the inferior-surface-of-tongue electrodes 111b, 112b, and 113b that correspond, respectively, and — (drawing abbreviation) are arranged by the column in X1, X2, —XN line. A vertical side electrode train is arranged by the set substrate 105 like the following.

[0035] In the process 2 of drawing 4 (a) and this drawing (b), the through holes 111e and 112e of the set substrate 105 and — are filled up with conductive members, such as electroconductive glue or solder, by screen-stencil etc. as fillers 111f and 112f. Next, electronic devices 111c and 112c and — are arranged in the top-face electrodes 111a and 112a and — by die bonding etc., respectively, and a pad is connected to approaching top-face electrode 113a of electronic devices 111c and 112c and —, and — by wirebonding etc. with Wires 111d and 112d.

[0036] In the process 3 of drawing 5 (a) and this drawing (b), adhesion loading of the metal mold 103 which has aperture 103a in the rim of the top face of the set substrate 105 is carried out.

[0037] In the process 4 of drawing 6 (a) and this drawing (b), it fills up with set closure resin (for example, epoxy system resin) 104 in aperture 103a of metal mold 103, and a cure is carried out. After cure hardening, if metal mold 103 is removed and dicing, a slicing machine, etc. cut set closure resin 104 and the set substrate 105 in the thickness direction according to the through hole train cut lines Y1 and Y2, —YN and the chip cut lines X1 and X2, —XN, the chip 100 of drawing 1 can be obtained.

[0038] Next, duplication in drawing 1 is avoided and the production process of other chips 150 by this invention is explained. In the process 1 of drawing 7 (a) and this drawing (b), the slot through holes 181 and 182 of the set substrate 155 and — are arranged on the constant spacing ****** through hole train cut lines Y1 and Y2 decided on a design, and —YN. Similarly, the top-face electrodes 161a and 162a and — are arranged in the constant spacing ****** chip cut lines X1 and X2 decided on a design, and —XN. It connects by the slot through holes 181 and 182 and —, and said top-face electrode and inferior-surface-of-tongue electrodes 161b and 162b, and — are arranged by the column in X1, X2, —XN line. A vertical side electrode train is arranged by the set substrate 155 like the following.

[0039] In the process 2 of drawing 8 (a) and this drawing (b), electronic devices 161c and 162c and — are arranged in the top-face electrodes 161a and 163a and — by die bonding etc., respectively, and a pad is connected to approaching top-face electrode 162a of electronic devices 161c and 162c and —, and — by wirebonding etc. with Wires 161d and 162d.

[0040] In the process 3 of drawing 9 (a) and this drawing (b), adhesion loading of the metal mold 153 which has aperture 153a in the top-face rim of the set substrate 155 is carried out.

[0041] In the process 4 of drawing 10 (a) and this drawing (b), it fills up with set closure resin (for example, epoxy system resin) 154 in aperture 153a of metal mold 153, and a cure is carried out. After cure hardening, if metal mold 153 is removed and dicing, a slicing

machine, etc. cut set closure resin 154 and the set substrate 155 in the thickness direction according to the through hole train cut lines Y1 and Y2, —YN and the chip cut lines X1 and X2, —XN, the slot through holes 181 and 182 can form the slot through hole sides 181a and 182a of a chip, and can obtain the chip 150 of drawing 2 .

[0042] Drawing 11 shows the fragmentary sectional view of the through hole section of the set substrate 105 of this invention, and through holes 111e and 112e and — are filled up with Fillers 111f and 112f and —. Moreover, the same is said of the fragmentary sectional view of the through hole section of other set substrates 155 by this invention, and the slot through holes 181 and 182 and — are filled up with Fillers 183a and 184a and —.

[0043] Moreover, by explanation of the gestalt of operation of this invention, it is at the end of a substrate. Although only one through hole and the vertical side electrode, and the chip that has one electronic device have been explained, you may be the chip which is not limited to this and has two or more through holes, and a vertical side electrode and two or more electronic devices at the end of a substrate.

[0044]

[Effect of the Invention] According to the configuration of this invention, since magnitude of closure resin and a substrate can be made the same, a micro surface mount mold chip can be obtained.

[0045] Since ** and a through hole are filled up with conductive members, such as electroconductive glue and solder, an influx to the through hole of closure resin can be prevented completely. Since a through hole is cut after ** and resin shaping, electrodes, such as flat solder, are formed in an end face. Therefore, defective continuity with a printed circuit board is not produced, either, but while connection becomes more certain, the solder fixed force also increases, and a very reliable surface mount mold chip can be obtained.

[0046] Furthermore, according to the manufacture approach of this invention, since set batch processing in several 100 pieces - 1000 number unit in a set substrate is possible and the chip of many surface mount molds can be manufactured from a set substrate, rational production can be realized, the large cost cut of a product is attained, and economical efficiency is very high.

[Translation done.]

* NOTICES *

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] Drawing 1 is the perspective view of the surface mount mold chip of this invention.
[Drawing 2] It is the perspective view of other surface mount mold chips by this invention.
[Drawing 3] (a) and (b) are the explanatory views of the main production processes 1 of the surface mount mold chip of this invention, this drawing (a) is a perspective view of a set substrate, and this drawing (b) is the fragmentary sectional view.
[Drawing 4] (a) and (b) are the explanatory views of the main production processes 2 of the surface mount mold chip of this invention, this drawing (a) is a perspective view of a set substrate, and this drawing (b) is the fragmentary sectional view.
[Drawing 5] (a) and (b) are the explanatory views of the main production processes 3 of the surface mount mold chip of this invention, this drawing (a) is a perspective view of a set substrate, and this drawing (b) is the fragmentary sectional view.
[Drawing 6] (a) and (b) are the explanatory views of the main production processes 4 of the surface mount mold chip of this invention, this drawing (a) is a perspective view of a set substrate, and this drawing (b) is the fragmentary sectional view.
[Drawing 7] (a) and (b) are the explanatory views of the main production processes 1 of other surface mount mold chips of this invention, and are this drawing. (a) is the perspective view of a set substrate and this drawing (b) is the fragmentary sectional view.
[Drawing 8] (a) and (b) are the explanatory views of the main production processes 2 of other surface mount mold chips of this invention, this drawing (a) is a perspective view of a set substrate, and this drawing (b) is the fragmentary sectional view.
[Drawing 9] (a) and (b) are the explanatory views of the main production processes 3 of other surface mount mold chips of this invention, this drawing (a) is a perspective view of a set substrate, and this drawing (b) is the fragmentary sectional view.
[Drawing 10] (a) and (b) are the explanatory views of the main production processes 4 of other surface mount mold chips of this invention, this drawing (a) is a perspective view of a set substrate, and this drawing (b) is the fragmentary sectional view.
[Drawing 11] It is the fragmentary sectional view of the through hole section of the set substrate of this invention.
[Drawing 12] It is the perspective view of the surface mount mold chip of the conventional example (1).
[Drawing 13] It is the perspective view of the surface mount mold chip of the conventional example (2).
[Drawing 14] (a) and (b) are the explanatory views of the main production processes 1 of the surface mount mold chip of the conventional example (1), this drawing (a) is a perspective view of a set substrate, and this drawing (b) is the fragmentary sectional view.
[Drawing 15] (a) and (b) are the explanatory views of the main production processes 2 of the surface mount mold chip of the conventional example (1), this drawing (a) is a perspective view of a set substrate, and this drawing (b) is the fragmentary sectional view.
[Drawing 16] (a) and (b) are the explanatory views of the main production processes 3 of the surface mount mold chip of the conventional example (1), this drawing (a) is a perspective view of a set substrate, and this drawing (b) is the fragmentary sectional view.
[Drawing 17] (a) and (b) are the explanatory views of the main production processes 4 of the surface mount mold chip of the conventional example (1), this drawing (a) is a perspective view of a set substrate, and this drawing (b) is the fragmentary sectional view.
[Drawing 18] (a) and (b) are the explanatory views of the main production processes 1 of the surface mount mold chip of the conventional example (2), this drawing (a) is a perspective view of a set substrate, and this drawing (b) is the fragmentary sectional view.
[Drawing 19] (a) and (b) are the explanatory views of the main production processes 2 of the surface mount mold chip of the conventional example (2), this drawing (a) is a perspective view of a set substrate, and this drawing (b) is the fragmentary sectional view.
[Drawing 20] (a) and (b) are the explanatory views of the main production processes 3 of the surface mount mold chip of the conventional example (2), this drawing (a) is a perspective view of a set substrate, and this drawing (b) is the fragmentary sectional view.
[Drawing 21] (a) and (b) are the explanatory views of the main production processes 4 of the surface mount mold chip of the conventional example (2), ** (a) is the perspective view of a set substrate, and this drawing (b) is the fragmentary sectional view.
[Drawing 22] It is the through hole section detail explanatory view of the set substrate cross section of the conventional example (1).
[Drawing 23] It is the through hole section detail explanatory view of the set substrate cross section of other conventional examples.
[Drawing 24] Furthermore, it is the through hole section detail explanatory view of the set substrate cross section of other conventional examples.
[Description of Notations]
100 150 Surface mount mold chip
101 151 Closure resin
104 154 Set closure resin
102 152 Substrate
111a, 112a, 161a, 162a Top-face electrode

111b, 112b, 161b, 162b Inferior-surface-of-tongue electrode
111c, 112c, 161c 162c Electronic device
111d, 112d, 161d, 162d Wire
111e, 112e Through hole
181 182 Slot through hole
181a, 182a Slot through hole side
111f, 112f, 183a, 184a Filler
105-155 Set substrate
103,153 Metal mold
X1, X2, --XN Through hole train cut line
Y1, Y2, --YN Chip cut line

[Translation done.]

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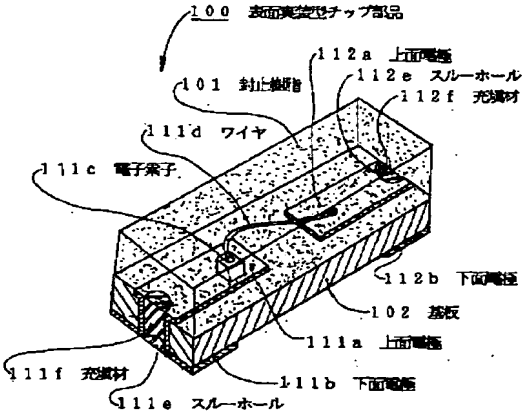
(54)【発明の名称】　表面実装型チップ部品及びその製造方法

(57)【要約】
【課題】　小形化が可能で、コスト／パフォーマンスの改善と高信頼性が図れる表面実装型チップ部品の構成と製造方法を提案する。
【解決手段】　導電性接着剤または半田等の導電部材で充填したスルーホールを有する複数の上下面電極を設けた集合基板に電子素子を配設し、電子素子を近接する電極に接続し、集合基板の上面側を封止樹脂でモールドし、封止樹脂と前記集合基板を同時に切断分割する製造方法からなる表面実装型チップ部品で、スルーホール部を含む上面側を樹脂封止することにより超小型の表面実装型チップ部品を得ることができる。



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【特許請求の範囲】

【請求項１】　スルーホールを有する複数の上下面電極を設けた紙フェノールまたはガラスエポキシ材等の集合基板の前記上面電極上に電子素子を配設し、該電子素子を前記上面電極と近接する電極にワイヤボンディング等で接続し、前記電子素子を前記集合基板上で封止樹脂でモールドし切断分割して構成された表面実装型チップ部品において、前記スルーホールを導電部材で充填して構成したことを特徴とする表面実装型チップ部品。

【請求項２】　前記導電部材は導電性接着剤、異方性導電接着剤、異方性導電シート、半田、銀ペーストの中の何れかひとつであることを特徴とする請求項１記載の表面実装型チップ部品。

【請求項３】　前記導電部材で充填された前記スルーホールと繋がる上面電極面側が前記封止樹脂でモールドされたことを特徴とする請求項１記載の表面実装型チップ部品。

【請求項４】　前記スルーホールが、前記表面実装型チップ部品の基板端面に形成されたことを特徴とする請求項１記載の表面実装型チップ部品。

【請求項５】　前記スルーホールが少なくとも一個以上基板の一端面に形成されたことを特徴とする請求項４記載の表面実装型チップ部品。

【請求項６】　スルーホールを有する複数の上下面電極を設けた紙フェノールまたはガラスエポキシ材等の集合基板の前記上面電極に電子素子を配設し、該電子素子を前記上面電極と近接する電極にワイヤボンディング等で接続し、前記電子素子を前記集合基板上で封止樹脂でモールドし切断分割して構成された表面実装型チップ部品の製造方法において、前記集合基板上にスルーホールを有する複数個の上下面電極を縦列横列に設ける工程と、前記スルーホールを導電部材で充填する工程と、前記電子素子を前記電極に配設する工程と、前記電子素子を近接する電極にワイヤボンディング等で接続する工程と、前記電子素子を前記集合基板上で封止樹脂でモールドする工程と、前記縦列横列に設けられたスルーホール列を前記モールドされた封止樹脂と共に前記基板厚み方向に切断する工程と、前記切断方向とほぼ直角方向に、封止樹脂と共に前記上下面電極列の外周部を前記集合基板の厚み方向に切断する工程とによって分割しチップ部品として形成することを特徴とする表面実装型チップ部品の製造方法。

【請求項７】　前記導電部材で充填された前記スルーホールと繋がる上面電極面側が前記封止樹脂でモールドされたことを特徴とする請求項６記載の表面実装型チップ部品の製造方法。

【請求項８】　前記スルーホールが、前記表面実装型チップ部品の基板端面に形成されたことを特徴とする請求項６記載の表面実装型チップ部品の製造方法。

【請求項９】　前記スルーホールが少なくとも一個以上

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基板の一端面に形成されたことを特徴とする請求項８記載の表面実装型チップ部品の製造方法。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は電子素子を樹脂モールドした電子部品に関する。更に詳しくは、プリント基板の表面実装に適した表面実装型チップ部品の構成及び製造方法に関する。

【０００２】

【従来の技術】基板の上面に電子素子を配設し、電子素子を含めて基板の上面側を封止樹脂でモールドした電子部品はよく知られている。また、電子機器の小形化薄形化傾向に従って、プリント基板へは表面実装が可能な電子部品、即ち表面実装型チップ部品が求められており、更に一層の小形化薄形化が期待されている。表面実装型チップ部品（以下チップ部品）は、直方体ブロックに近い形をしており、その底面または底面に近い側面に電極端子があり、プリント基板上の配線パターンに配設され、その配線パターンと接した電極端子とを導電性接着剤で容易に接続できる構成になっている場合が多い。以下では、従来例のチップ部品の構成と製造方法について説明する。

【０００３】図１２は従来例（１）のチップ部品の斜視図である。図１３は従来例（２）のチップ部品の斜視図である。図１４（ａ），（ｂ）～図１７（ａ），（ｂ）は従来例（１）の主な製造工程１～４の説明図で、同図（ａ）は集合基板の斜視図、同図（ｂ）はその部分断面図ある。図１８（ａ），（ｂ）～図２１（ａ），（ｂ）は従来例（２）の主な製造工程１～４の説明図で、同図（ａ）は集合基板の斜視図、同図（ｂ）はその部分断面図ある。図２２～図２４は従来例の集合基板断面のスルーホール部詳細説明図である。

【０００４】図１２において、チップ部品２００は例えば紙フエノール材、ガラスエポキシ材等の基板２０２と、基板２０２の上面にモールドされた封止樹脂２０１とで構成される。基板２０２には銅箔がエッチング等で形成された上面電極２１１ａ、２１２ａ及び下面電極２１１ｂ、２１２ｂが設けられ、上面電極２１１ａ、２１２ａ及び下面電極２１１ｂ、２１２ｂは夫々スルーホール２１１ｅ　、２１２ｅによって接続されている。そして、前記スルーホール２１１ｅ、２１２ｅは後述するスルーホールを連ねたスルーホール列カット線上にあって、ほぼその中心に沿って、基板２０２の厚み方向に切断されてその断面はほぼ半円形に形成されている。例えば、発光または受光素子からなる電子素子２１１ｃは、上面電極２１１ａにダイボンディング等によって配設され、電子素子２１１ｃのパッドはボンディングワイヤ２１１ｄによって近接する上面電極２１２ａに接続される。又、封止樹脂２０１はスルーホール２１１ｅ、２１２ｅにモールド時に樹脂が流れ込むのを避けることや、

流れ込んだ樹脂がキュア後硬化して下面電極２１１ｂ、２１２ｂの表面を覆ってプリント基板との間で導通不良が生じるのを避けるために、スルーホール２１１ｅ、２１２ｅより離して設けられている。従って、基板２０２は封止樹脂２０１の大きさより大きくする必要があり、チップ部品の小型化を困難にしていた。

【０００５】図１３においてチップ部品２５０は、重複を避けて図１２との相違点のみを説明すれば、後述する長穴スルーホールから形成される長穴スルーホール辺２８１ａ、２８２ａが基板２５２の両端に設けられる。上面電極２５１ａ、２５２ａ、下面電極２５１ｂ、２５２ｂ、長穴スルーホール辺２８１ａ、２８２ａとの配設関係は図１２と同様である。この場合も、図１２と同様に、封止樹脂２５１はスルーホール辺２８１ａ、２８２ａにモールド時に樹脂が流れ込むのを避けるために、スルーホール辺２８１ａ、２８２ａより離して設けられている。従って、基板２５２は封止樹脂２５１の大きさより大きくする必要があり、同様に、チップ部品の小型化を困難にしていた。

【０００６】次に、従来例（１）の製造方法について説明する。図１４（ａ）及び同図（ｂ）の工程１において、集合基板２０５のスルーホールは設計上決まる定間隔離れたスルーホール列カット線Ｙ１、Ｙ２、…ＹＮ上に配置される。同様に、前記上下面電極は設計上決まる定間隔離れたチップカット線Ｘ１、Ｘ２、…ＸＮ内に配設される。上面電極２１１ａ、２１２ａ、２１３ａ…及びそれらと夫々対応する下面電極２１１ｂ、２１２ｂ、２１３ｂ、…（図省略）は、スルーホール２１１ｅ、２１２ｅ，２１３ｅ、…で接続されてＸ１，Ｘ２線内に縦列に配設される。以下同様にして上下面電極列が集合基板２０５に配設される。

【０００７】図１５（ａ）及び同図（ｂ）の工程２において、電子素子２１１ｃ、２１２ｃ、…は夫々上面電極２１１ａ、２１２ａ、…にダイボンディング等で配設され、電子素子２１１ｃ、２１２ｃ、…のパッドは、近接する上面電極２１３ａ、…にワイヤ２１１ｄ、２１２ｄでワイヤボンディング等によって接続される。

【０００８】図１６（ａ）及び同図（ｂ）の工程３において、集合基板２０５の上面に、窓枠２０３ａ、２０３ｂ、２０３ｃ、…を有する金型２０３が前記スルーホール列を覆うように、接着搭載される。

【０００９】図１７（ａ）及び同図（ｂ）の工程４において、金型２０３内に集合封止樹脂（例えばエポキシ系樹脂）２０４ａ、２０４ｂ、２０４ｃが充填されてキュアされる。キュア硬化後、金型２０３を外してスルーホール列カット線Ｙ１、Ｙ２、…ＹＮ及びチップカット線Ｘ１、Ｘ２、…ＸＮに従って集合基板２０５を厚み方向にダイシング、スライシングマシン等で切断すれば、図１２のチップ部品２００を得ることができる。

【００１０】次に従来例（２）を示す製造工程を、従来例（１）との重複を避けて説明する。図１８（ａ）及び同図（ｂ）の工程１において、集合基板２５５の長穴スルーホール２８１、２８２、…は設計上決まる定間隔離れた位置に配置される。同様に、上面電極２６１ａ、２６２ａ、…は設計上決まる定間隔離れたチップカット線Ｘ１、Ｘ２、…ＸＮ内に配設され、前記上面電極と下面電極２６１ｂ、２６２ｂ…は、長穴スルーホール２８１、２８２、…で接続されてＸ１、Ｘ２線内に縦列に配設される。以下同様にして上下面電極列が集合基板２５５に配設される。

【００１１】図１９（ａ）及び同図（ｂ）の工程２において、電子素子２６１ｃ、２６２ｃ…は夫々上面電極２６１ａ、２６３ａ、…にダイボンディング等で配設され、電子素子２６１ｃ、２６２ｃ、…のパッドは、近接する上面電極２６２ａ、…にワイヤ２６１ｄ、２６２ｄでワイヤボンディング等によって接続される。

【００１２】図２０（ａ）及び同図（ｂ）の工程３において、集合基板２５５の上面に、窓枠２５３ａ、２５３ｂ、…を有する金型２５３が長穴スルーホール２８１、２８２を覆うように、接着搭載される。

【００１３】図２１（ａ）及び同図（ｂ）の工程４において、金型２５３内に集合封止樹脂（例えばエポキシ系樹脂）２５４ａ、２５４ｂが充填されてキュアされる。キュア硬化後に金型２５３を外してチップカット線Ｘ１、Ｘ２、…ＸＮに従って集合基板２５５を厚み方向にダイシング、スライシングマシン等で切断すれば、長穴スルーホール２８１、２８２はチップ部品の長穴スルーホール辺２８１ａ、２８２ａを形成して図１３のチップ部品２５０を得ることができる。

【００１４】図２２は従来例（１）の集合基板２０５の断面のスルーホール部詳細説明図を示すもので、金型２０３がスルーホール２１１ｅ、２１２ｅ、…をふさいでいるので封止樹脂２０４ａ、２０４ｂ、…の流れ込みは生じない。従来例（２）の集合基板２５５の長穴スルーホールについても同様なので説明を省略する。

【００１５】図２３は、もう一つの従来例であり、レジスト２９０によってスルーホール２９１がふさがれているので封止樹脂２９３の流れ込みは生じない。

【００１６】図２４は、更にもう一つの従来例であり、電極と同じ銅箔やメッキ材２９４でスルーホール２９１がふさがれているので封止樹脂２９３の流れ込みは生じない。

【００１７】

【発明が解決しようとする課題】しかしながら、従来のチップ部品には以下のような問題があった。従来例（１）では、図１２に示すように封止樹脂２０１がスルーホール２１１ｅ　、２１２ｅにモールド時に流れこむのを避けるためや、流れ込んだ樹脂がキュア後硬化して下面電極とプリント基板との間の導通不良が生ずるのを避けるために、スルーホール２１１ｅ、２１２ｅを封止

樹脂２０１から離す必要がある。その結果、封止樹脂２０１の大きさより基板２０２の方が大きく形成されている。このために、チップ部品の小形化が困難であり、また基板が大きい分だけ材料費が掛り、コスト／パフォーマンスが改善されなかった。

【００１８】また、従来例（２）の場合も、上記従来例（１）の場合と同様の理由により、長穴スルーホール２８１、２８２は封止樹脂２５１から離す必要がある。その結果、封止樹脂２５１の大きさより基板２５２の方が大きく形成されている。スルーホールが長穴となり、製造工程はやや簡略化されてはいるものの、課題として上記従来例（１）と同様、チップ部品の小形化が困難であり、また基板が大きい分だけ材料費が掛り、コスト／パフォーマンスが改善されなかった。

【００１９】また、別の従来例を示すスルーホール部の部分断面図、図２３では、レジスト２９０の蓋があるので封止樹脂２９３のスルーホール２９１への流れ込みは生じないものの、レジスト２９０の下面部分で生じる気泡２９２が抜けず、上面電極と下面電極をメッキで接続することができず、導通不良が発生するという問題があった。

【００２０】また、もう一つの従来例を示すスルーホール部の部分断面図、図２４では、電極と同じ銅箔やメッキ材２９４の蓋があるので、封止樹脂２９３のスルーホール２９１への流れ込みは生じないものの、電極と同じ銅箔やメッキ材２９４の下面部分で生じる気泡２９２が抜けず、上記従来例と同様に、上面電極と下面電極をメッキで接続することができず、導通不良が発生するという問題があった。

【００２１】本発明の目的は、前述の欠点を除去して、小形薄形化が可能で信頼性の高い表面実装型チップ部品とその製造方法を提案するものである。

【００２２】

【課題を解決するための手段】上記目的を達成するために、本発明における表面実装型チップ部品はスルーホールを有する複数の上下面電極を設けた紙フェノールまたはガラスエポキシ材等の集合基板の前記上面電極上に電子素子を配設し、該電子素子を前記上面電極と近接する電極にワイヤボンディング等で接続し、前記電子素子を前記集合基板上で封止樹脂でモールドし切断分割して構成された表面実装型チップ部品において、前記スルーホールを導電部材で充填して構成したことを特徴とするものである。

【００２３】また、前記導電部材は導電性接着剤、異方性接着剤、異方性導電シート、半田、銀ペーストの中の何れかひとつであることを特徴とするものである。

【００２４】また、前記導電部材で充填された前記スルーホールと繋がる上面電極面側が前記封止樹脂でモールドされたことを特徴とするものである。

【００２５】また、前記スルーホールが、前記表面実装型チップ部品の基板端面に形成されたことを特徴とするものである。

【００２６】また、前記スルーホールが少なくとも一個以上基板の一端面に形成されたことを特徴とするものである。

【００２７】また、本発明における表面実装型チップ部品の製造方法はスルーホールを有する複数の上下面電極を設けた紙フェノールまたはガラスエポキシ材等の集合基板の前記上面電極に電子素子を配設し、該電子素子を前記上面電極と近接する電極にワイヤボンディング等で接続し、前記電子素子を前記集合基板上で封止樹脂でモールドし切断分割して構成された表面実装型チップ部品の製造方法において、前記集合基板上にスルーホールを有する複数個の上下面電極を縦列横列に設ける工程と、前記スルーホールを導電部材で充填する工程と、前記電子素子を前記電極に配設する工程と、前記電子素子を近接する電極にワイヤボンディング等で接続する工程と、前記電子素子を前記集合基板上で封止樹脂でモールドする工程と、前記縦列横列に設けられたスルーホール列を前記モールドされた封止樹脂と共に前記基板厚み方向に切断する工程と、前記切断方向とほぼ直角方向に、封止樹脂と共に前記上下面電極列の外周部を前記集合基板の厚み方向に切断する工程とによって分割しチップ部品として形成することを特徴とするものである。

【００２８】また、本発明の製造方法は前記導電部材で充填された前記スルーホールと繋がる上面電極面側が前記封止樹脂でモールドされたことを特徴とするものである。

【００２９】また、本発明の製造方法は前記スルーホールが、前記表面実装型チップ部品の基板端面に形成されたことを特徴とするものである。

【００３０】また更に、本発明の製造方法は前記スルーホールが少なくとも一個以上基板の一端面に形成されたことを特徴とするものである。

【００３１】

【発明の実施の形態】以下では、本発明の実施の形態を図面に基づいて説明する。図１は本発明のチップ部品の斜視図である。図２は本発明による他のチップ部品の斜視図である。図３（ａ）、（ｂ）～図６（ａ）、（ｂ）は本発明のチップ部品の主な製造工程１～４の説明図で、同図（ａ）は集合基板の斜視図、同図（ｂ）はその断面図である。図７（ａ）、（ｂ）～図１０（ａ）、（ｂ）は本発明による他のチップ部品の主な製造工程１～４の説明図で、同図（ａ）は集合基板の斜視図、同図（ｂ）はその断面図である。図１１は本発明を示す集合基板断面のスルーホール部詳細説明図である。

【００３２】図１において、本発明のチップ部品１００は例えばガラスエポキシ材等の基板１０２と、基板１０２の上面にモールドされた封止樹脂１０１とで構成される。基板１０２には銅箔がエッチング等で形成された上

面電極１１１ａ、１１２ａ及び下面電極１１１ｂ、１１２ｂが設けられ、上面電極１１１ａ、１１２ａ及び下面電極１１１ｂ、１１２ｂは夫々スルーホール１１１ｅ、１１２ｅによって接続されている。そして、スルーホール１１１ｅ、１１２ｅは後述するスルーホール列カット線上にあって、ほぼ中心に沿って、基板１０２の厚み方向に切断されてその断面はほぼ半円形に形成されている。例えば、発光または受光素子からなる電子素子１１１ｃは、上面電極１１１ａにダイボンディングによって配設され、電子素子１１１ｃのパッドはボンディングワイヤ１１１ｄによって近接する上面電極１１２ａに接続される。又、スルーホール１１１ｅ、１１２ｅには導電性接着剤または半田等の導電部材がスクリーン印刷等により充填材１１１ｆ、１１２ｆとして充填されている。尚、導電部材としては、前記の物のほかに異方性導電接着剤、異方性導電シート、銀ペースト等の中より適宜選ぶことができる。

【００３３】図２において、本発明のチップ部品１５０は、重複を避けて図１との相違点のみを説明すれば、後述する長穴スルーホール辺１８１ａ、１８２ａが基板１５２の両端に設けられる。上面電極１６１ａ、１６２ａ、下面電極１６１ｂ、１６２ｂ、長穴スルーホール辺１８１ａ、１８２ａとの配設関係は図１と同様である。尚、長穴スルーホール辺１８１ａ、１８２ａには導電接着剤または半田等の導電部材がスクリーン印刷等により充填材１８３ａ、１８４ａとして充填されている。

【００３４】次に、本発明のチップ部品１００の製造方法について説明する。図３（ａ）及び同図（ｂ）の工程１において、集合基板１０５のスルーホールは設計上決まる定間隔離れたスルーホール列カット線Ｙ１、Ｙ２、…ＹＮ上に配置される。同様に、前記上下面電極は設計上決まる定間隔離れたチップカット線Ｘ１、Ｘ２、…ＸＮ内に配設される。上面電極１１１ａ、１１２ａ、１１３ａ、…及びそれらと夫々対応する下面電極１１１ｂ、１１２ｂ、１１３ｂ、…（図省略）は、スルーホール１１１ｅ、１１２ｅ、…で接続されてＸ１、Ｘ２、…ＸＮ線内に縦列に配設される。以下同様にして上下面電極列が集合基板１０５に配設される。

【００３５】図４（ａ）及び同図（ｂ）の工程２において、集合基板１０５のスルーホール１１１ｅ、１１２ｅ、…に導電性接着剤または半田等の導電部材がスクリーン印刷等により充填材１１１ｆ、１１２ｆとして充填される。次に、電子素子１１１ｃ、１１２ｃ、…が夫々上面電極１１１ａ、１１２ａ、…にダイボンディング等で配設され、電子素子１１１ｃ、１１２ｃ、…のパッドは、近接する上面電極１１３ａ、…にワイヤ１１１ｄ、１１２ｄでワイヤボンディング等によって接続される。

【００３６】図５（ａ）及び同図（ｂ）の工程３において、集合基板１０５の上面の外縁に、窓１０３ａを有する金型１０３が接着搭載される。

【００３７】図６（ａ）及び同図（ｂ）の工程４において、集合封止樹脂（例えばエポキシ系樹脂）１０４が金型１０３の窓１０３ａ内に充填されてキュアされる。キュア硬化後、金型１０３を外してスルーホール列カット線Ｙ１、Ｙ２、…ＹＮ及びチップカット線Ｘ１、Ｘ２、…ＸＮに従って集合封止樹脂１０４及び集合基板１０５を厚み方向にダイシング、スライシングマシン等で切断すれば、図１のチップ部品１００を得ることができる。

【００３８】次に本発明による他のチップ部品１５０の製造工程を、図１との重複を避けて説明する。図７（ａ）及び同図（ｂ）の工程１において、集合基板１５５の長穴スルーホール１８１、１８２、…は設計上決まる定間隔離れたスルーホール列カット線Ｙ１、Ｙ２、…ＹＮ上に配設される。同様に、上面電極１６１ａ、１６２ａ、…は設計上決まる定間隔離れたチップカット線Ｘ１、Ｘ２、…ＸＮ内に配設され　、前記上面電極と下面電極１６１ｂ、１６２ｂ、…は、長穴スルーホール１８１、１８２、…で接続されてＸ１、Ｘ２、…ＸＮ線内に縦列に配設される。以下同様にして上下面電極列が集合基板１５５に配設される。

【００３９】図８（ａ）及び同図（ｂ）の工程２において、電子素子１６１ｃ、１６２ｃ、…は夫々上面電極１６１ａ、１６３ａ、…にダイボンディング等で配設され、電子素子１６１ｃ、１６２ｃ、…のパッドは、近接する上面電極１６２ａ、…にワイヤ１６１ｄ、１６２ｄでワイヤボンディング等で接続される。

【００４０】図９（ａ）及び同図（ｂ）の工程３において、集合基板１５５の上面外縁に、窓１５３ａを有する金型１５３が接着搭載される。

【００４１】図１０（ａ）及び同図（ｂ）の工程４において、集合封止樹脂（例えばエポキシ系樹脂）１５４が金型１５３の窓１５３ａ内に充填されてキュアされる。キュア硬化後、金型１５３を外してスルーホール列カット線Ｙ１、Ｙ２、…ＹＮ及びチップカット線Ｘ１、Ｘ２、…ＸＮに従って集合封止樹脂１５４及び集合基板１５５を厚み方向にダイシング、スライシングマシン等で切断すれば、長穴スルーホール１８１、１８２はチップ部品の長穴スルーホール辺１８１ａ、１８２ａを形成して図２のチップ部品１５０を得ることができる。

【００４２】図１１は本発明の集合基板１０５のスルーホール部の部分断面図を示すもので、スルーホール１１１ｅ、１１２ｅ、…は充填材１１１ｆ、１１２ｆ、…で充填されている。また、本発明による他の集合基板１５５のスルーホール部の部分断面図についても同様であり、長穴スルーホール１８１、１８２、…は充填材１８３ａ、１８４ａ、…で充填されている。

【００４３】また、本発明の実施の形態の説明では、基板の一端に　一つのスルーホール及び上下面電極と１個の電子素子を有するチップ部品についてのみ説明してきたが、これに限定されることはなく、基板の一端に複数

個のスルーホールや上下面電極及び複数個の電子素子を有するチップ部品であってもよい。

【００４４】

【発明の効果】本発明の構成によれば、封止樹脂と基板の大きさを同一にできるため、超小型の表面実装型チップ部品を得ることができる。

【００４５】又、スルーホールは導電性接着剤や半田等の導電部材で充填されているので、封止樹脂のスルーホールへの流れ込みは完全に防止できる。又、樹脂成形後にスルーホールがカットされるのでフラットな半田等の電極が端面に形成される。そのために、プリント基板との導通不良も生ぜず、接続がより確実になると同時に半田固定力も増加し、信頼性が極めて高い表面実装型チップ部品を得ることができる。

【００４６】更に、本発明の製造方法によれば、集合基板での、数１００個～数１０００個単位での集合一括処理が可能なために集合基板から多数の表面実装型のチップ部品が製造できるので、合理的生産が実現でき、製品の大幅なコストダウンが可能となり、経済性が極めて高い。

【図面の簡単な説明】

【図１】図１は本発明の表面実装型チップ部品の斜視図である。

【図２】本発明による他の表面実装型チップ部品の斜視図である。

【図３】（ａ）、（ｂ）は本発明の表面実装型チップ部品の主な製造工程１の説明図で、同図（ａ　）は集合基板の斜視図、同図（ｂ）はその部分断面図である。

【図４】（ａ）、（ｂ）は本発明の表面実装型チップ部品の主な製造工程２の説明図で、同図（ａ　）は集合基板の斜視図、同図（ｂ）はその部分断面図である。

【図５】（ａ）、（ｂ）は本発明の表面実装型チップ部品の主な製造工程３の説明図で、同図（ａ　）は集合基板の斜視図、同図（ｂ）はその部分断面図である。

【図６】（ａ）、（ｂ）は本発明の表面実装型チップ部品の主な製造工程４の説明図で、同図（ａ　）は集合基板の斜視図、同図（ｂ）はその部分断面図である。

【図７】（ａ）、（ｂ）は本発明の他の表面実装型チップ部品の主な製造工程１の説明図で、同図　（ａ）は集合基板の斜視図、同図（ｂ）はその部分断面図である。

【図８】（ａ）、（ｂ）は本発明の他の表面実装型チップ部品の主な製造工程２の説明図で、同図（ａ）は集合基板の斜視図、同図（ｂ）はその部分断面図である。

【図９】（ａ）、（ｂ）は本発明の他の表面実装型チップ部品の主な製造工程３の説明図で、同図（ａ）は集合基板の斜視図、同図（ｂ）はその部分断面図である。

【図１０】（ａ）、（ｂ）は本発明の他の表面実装型チップ部品の主な製造工程４の説明図で、同図（ａ）は集合基板の斜視図、同図（ｂ）はその部分断面図である。

【図１１】本発明の集合基板のスルーホール部の部分断面図である。

【図１２】従来例（１）の表面実装型チップ部品の斜視図である。

【図１３】従来例（２）の表面実装型チップ部品の斜視図である。

【図１４】（ａ）、（ｂ）は従来例（１）の表面実装型チップ部品の主な製造工程１の説明図で、同図（ａ）は集合基板の斜視図、同図（ｂ）はその部分断面図である。

【図１５】（ａ）、（ｂ）は従来例（１）の表面実装型チップ部品の主な製造工程２の説明図で、同図（ａ）は集合基板の斜視図、同図（ｂ）はその部分断面図である。

【図１６】（ａ）、（ｂ）は従来例（１）の表面実装型チップ部品の主な製造工程３の説明図で、同図（ａ）は集合基板の斜視図、同図（ｂ）はその部分断面図である。

【図１７】（ａ）、（ｂ）は従来例（１）の表面実装型チップ部品の主な製造工程４の説明図で、同図（ａ）は集合基板の斜視図、同図（ｂ）はその部分断面図である。

【図１８】（ａ）、（ｂ）は従来例（２）の表面実装型チップ部品の主な製造工程１の説明図で、同図（ａ）は集合基板の斜視図、同図（ｂ）はその部分断面図である。

【図１９】（ａ）、（ｂ）は従来例（２）の表面実装型チップ部品の主な製造工程２の説明図で、同図（ａ）は集合基板の斜視図、同図（ｂ）はその部分断面図である。

【図２０】（ａ）、（ｂ）は従来例（２）の表面実装型チップ部品の主な製造工程３の説明図で、同図（ａ）は集合基板の斜視図、同図（ｂ）はその部分断面図である。

【図２１】（ａ）、（ｂ）は従来例（２）の表面実装型チップ部品の主な製造工程４の説明図で、同（ａ）は集合基板の斜視図、同図（ｂ）はその部分断面図である。

【図２２】従来例（１）の集合基板断面のスルーホール部詳細説明図である。

【図２３】他の従来例の集合基板断面のスルーホール部詳細説明図である。

【図２４】更に他の従来例の集合基板断面のスルーホール部詳細説明図である。

【符号の説明】

１００、１５０　表面実装型チップ部品
１０１、１５１　封止樹脂
１０４、１５４　集合封止樹脂
１０２、１５２　基板
１１１ａ、１１２ａ、１６１ａ、１６２ａ　上面電極
１１１ｂ、１１２ｂ、１６１ｂ、１６２ｂ　下面電極
１１１ｃ、１１２ｃ、１６１ｃ　１６２ｃ　電子素子

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１１１ｄ、１１２ｄ、１６１ｄ、１６２ｄ　ワイヤ
１１１ｅ、１１２ｅ　スルーホール
１８１、１８２　長穴スルーホール
１８１ａ、１８２ａ　長穴スルーホール辺
１１１ｆ、１１２ｆ、１８３ａ、１８４ａ　充填材　＊

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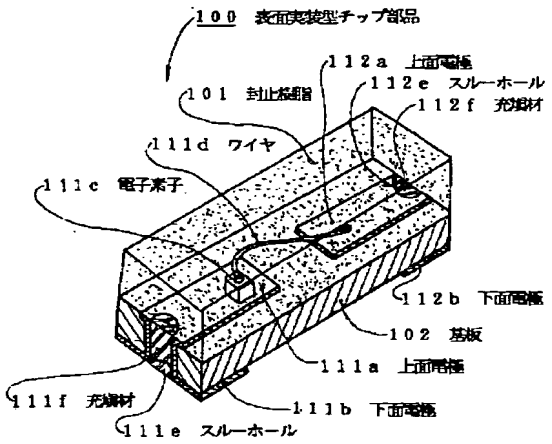
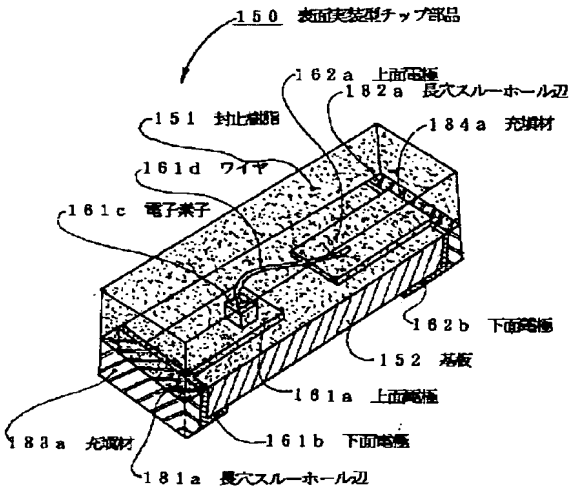
＊１０５、１５５　集合基板
１０３，１５３　金型
Ｘ１、Ｘ２、…ＸＮ　スルーホール列カット線
Ｙ１、Ｙ２、…ＹＮ　チップカット線

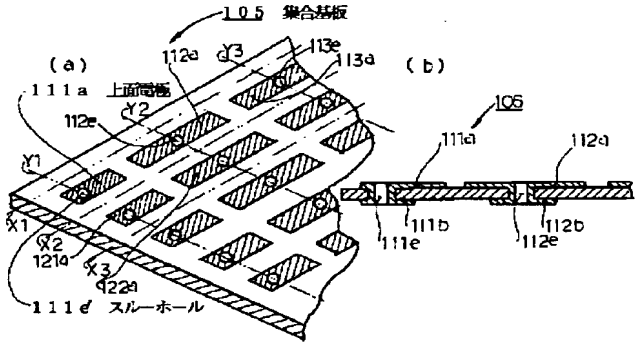
【図１】



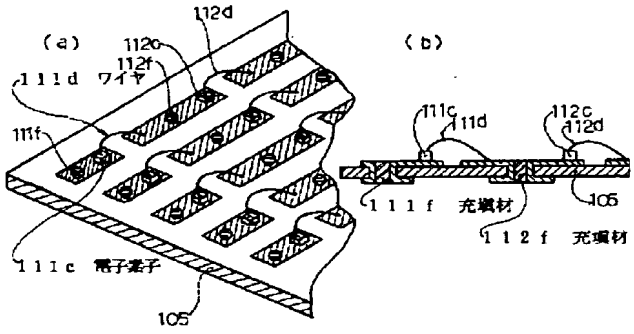
【図２】



【図３】



【図４】



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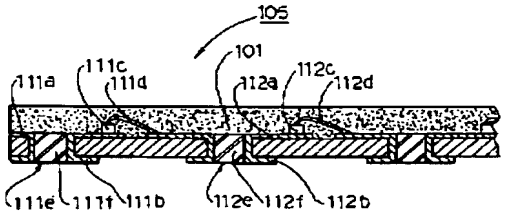

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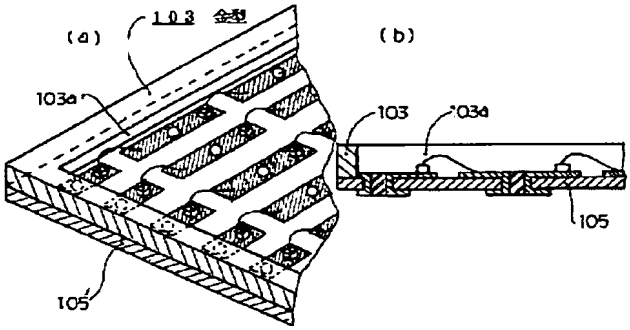

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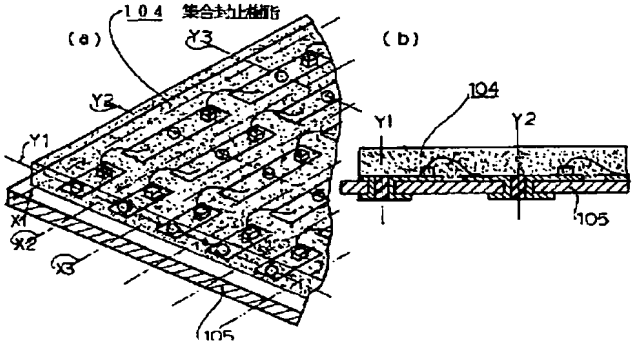

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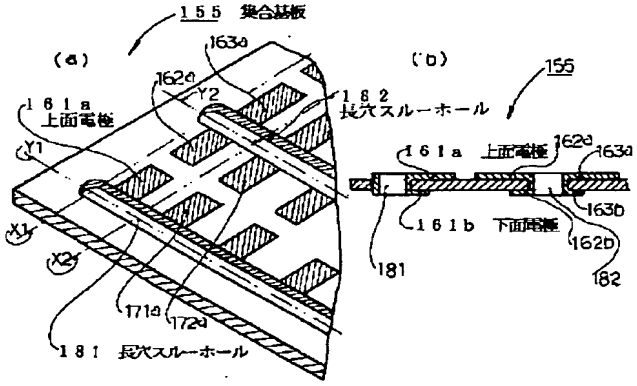

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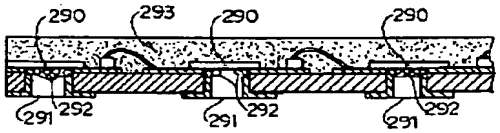

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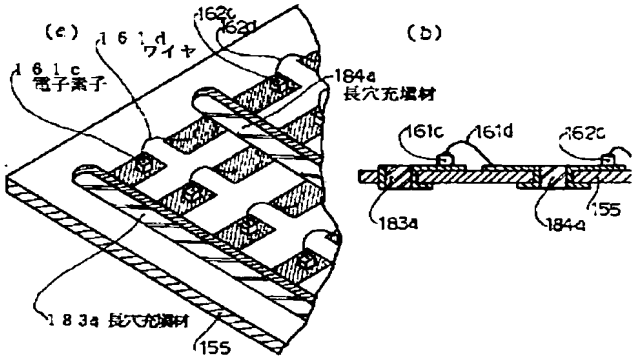

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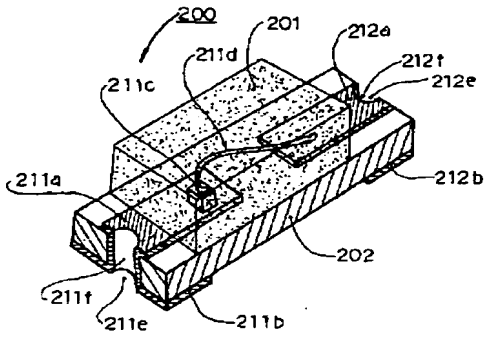

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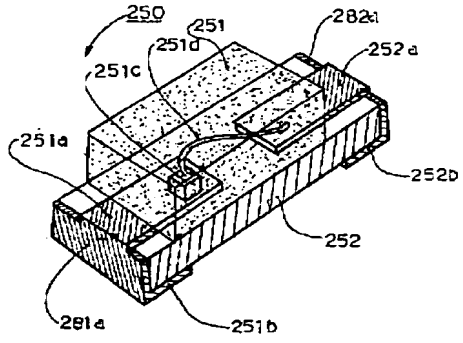

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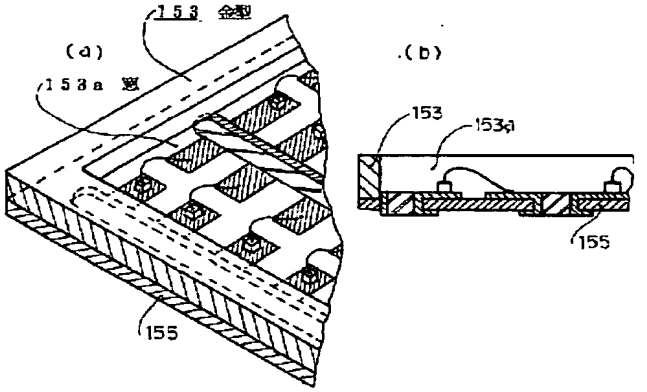

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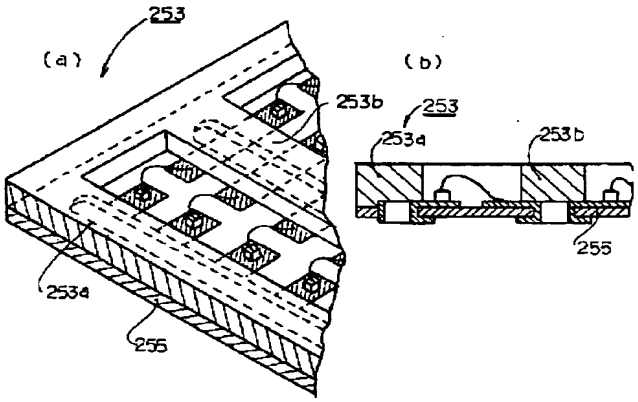

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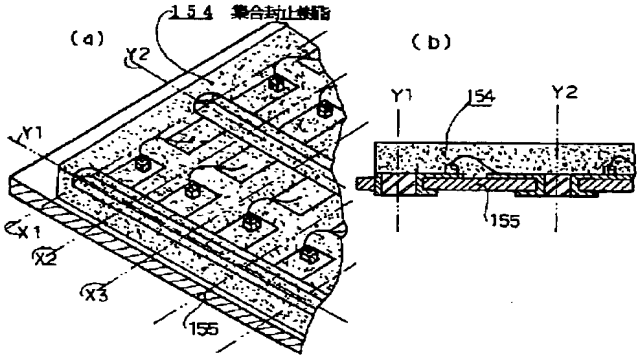

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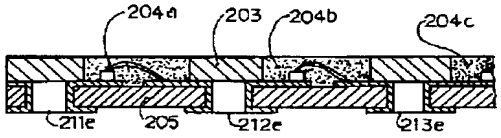

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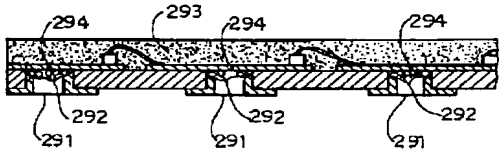

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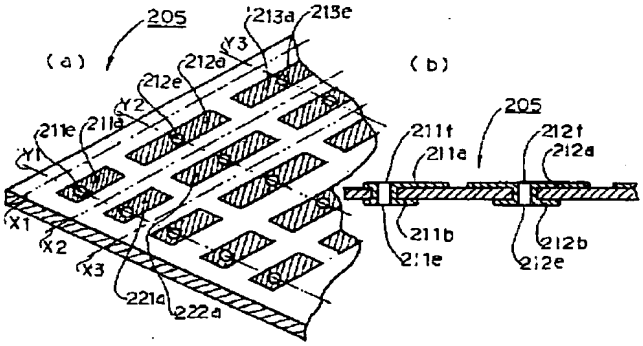

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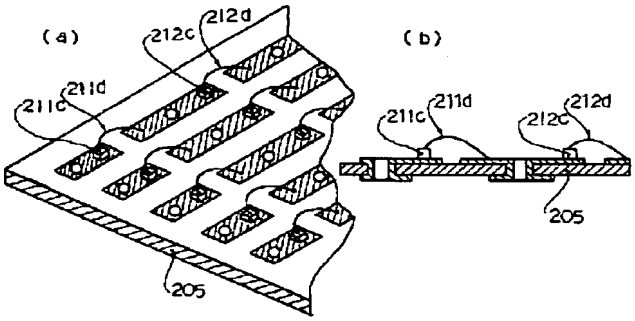
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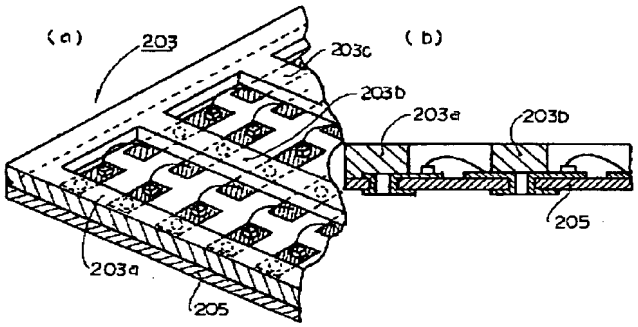
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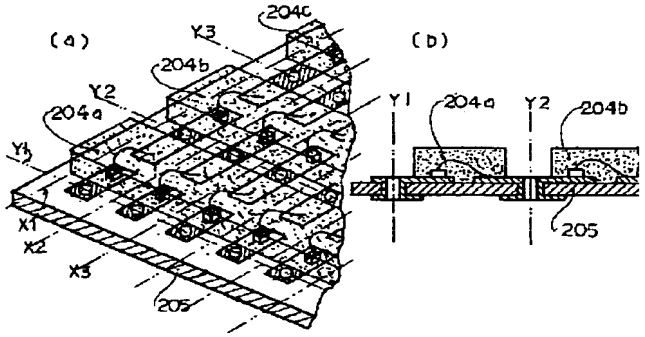
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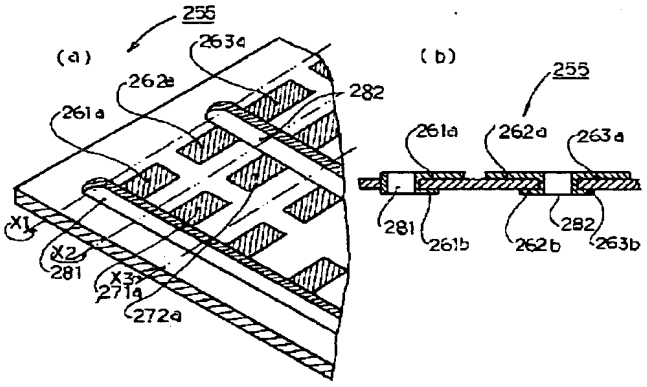
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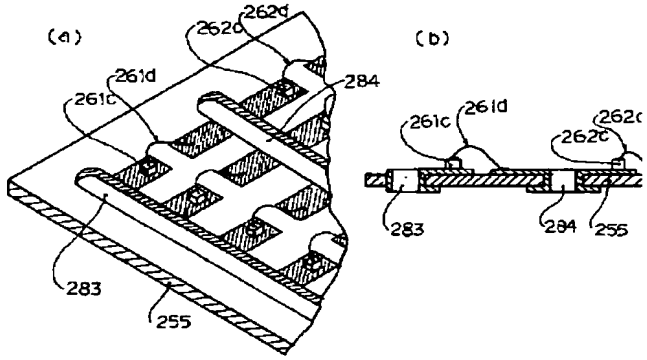
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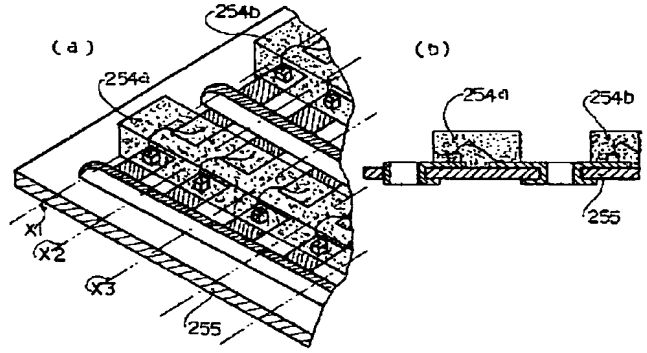
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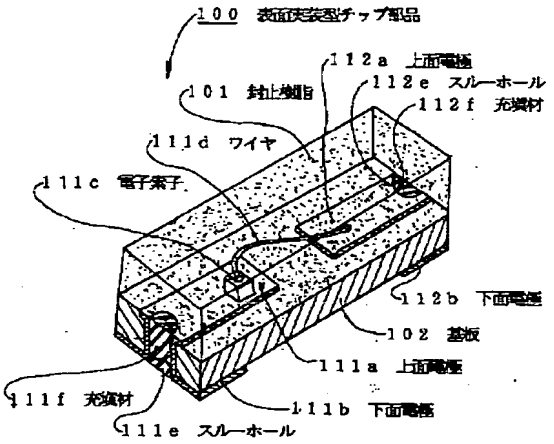
【手続補正書】
【提出日】平成９年１２月２日
【手続補正１】
【補正対象書類名】図面　＊
＊【補正対象項目名】全図
【補正方法】変更
【補正内容】

【図１】



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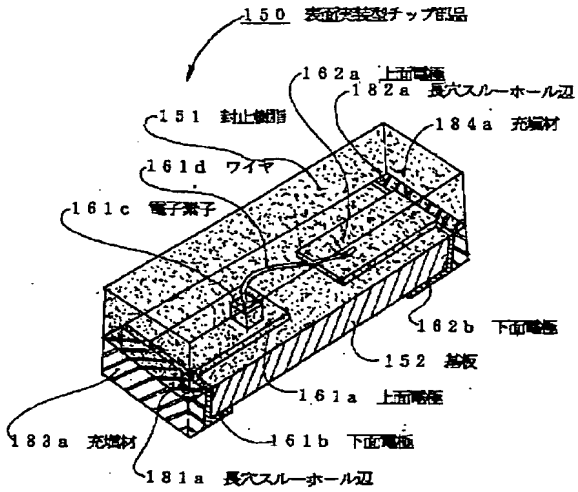

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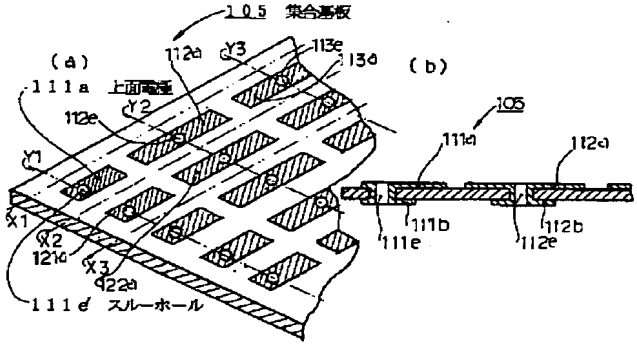

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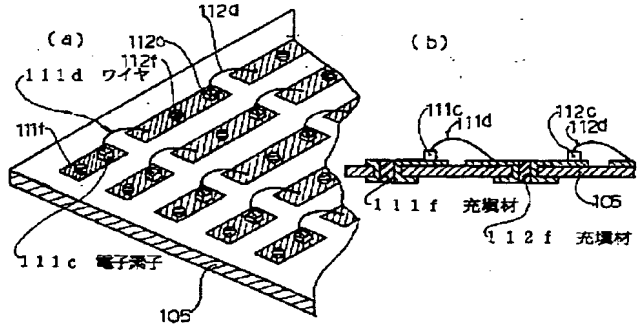

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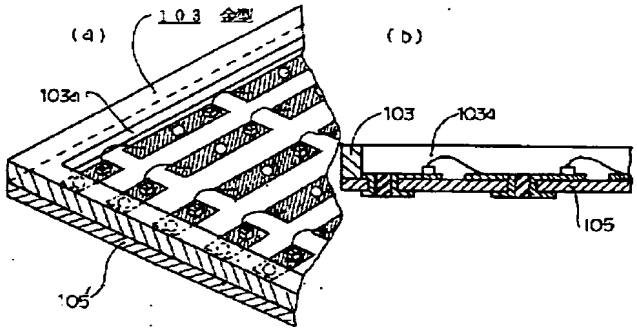

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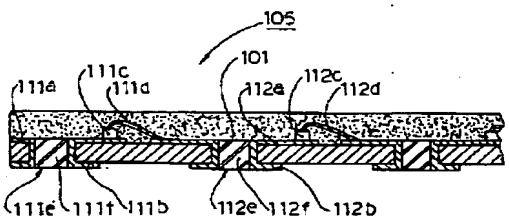

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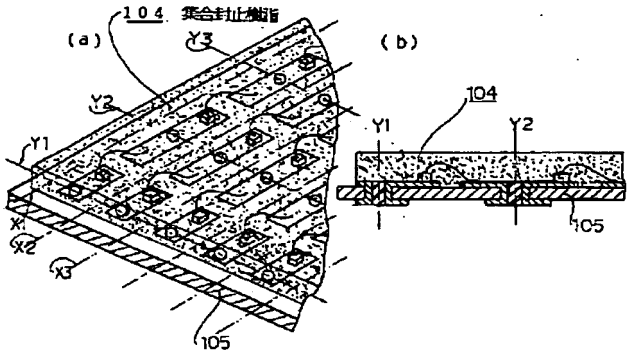

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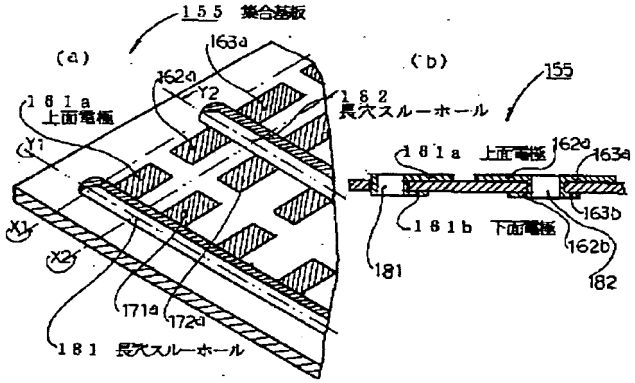

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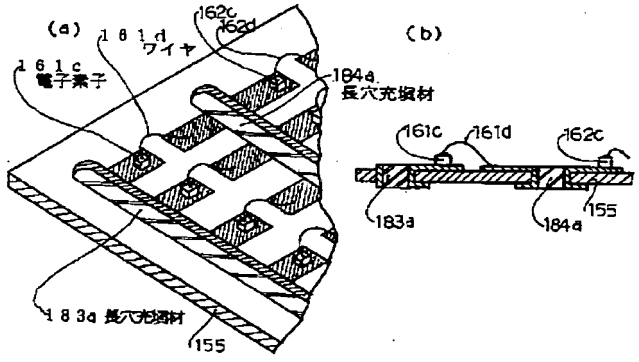

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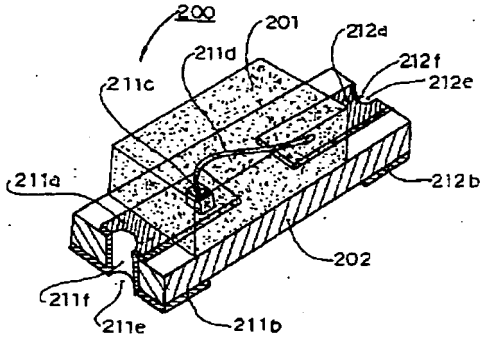

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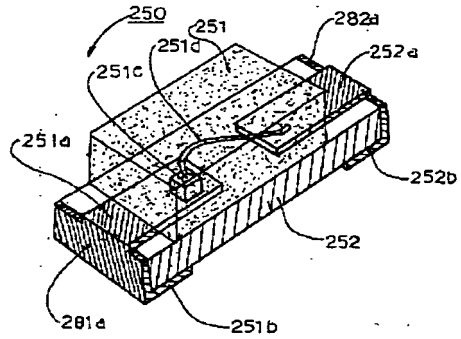

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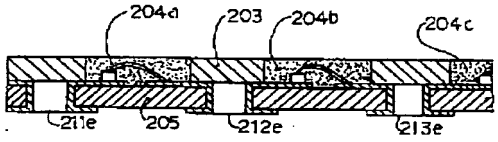

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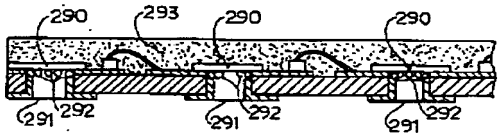

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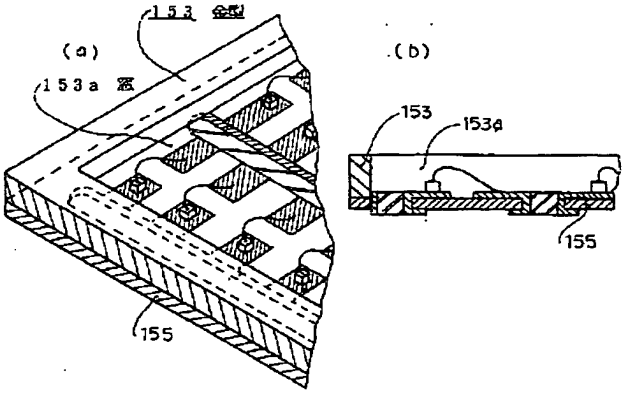

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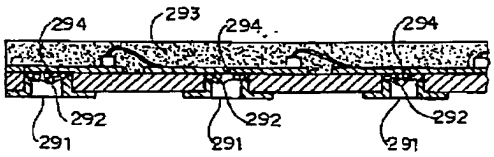

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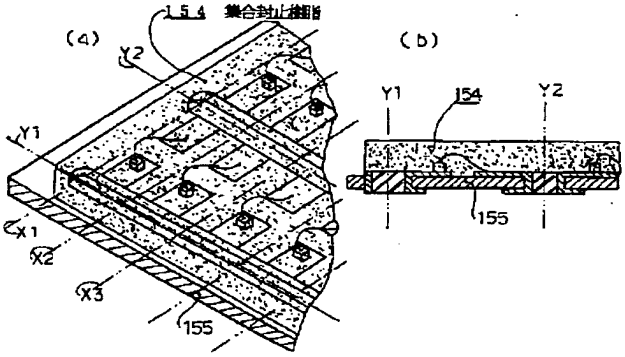

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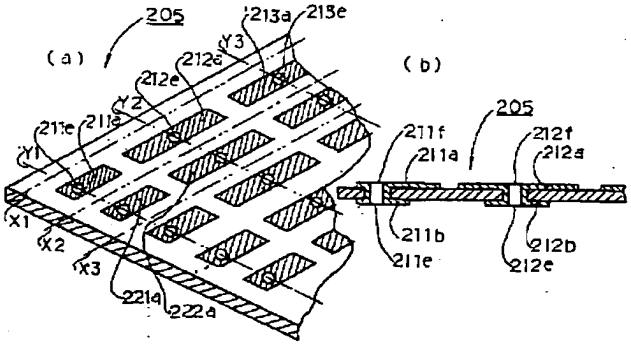

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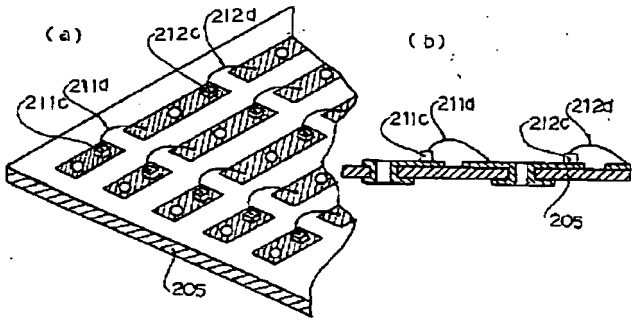
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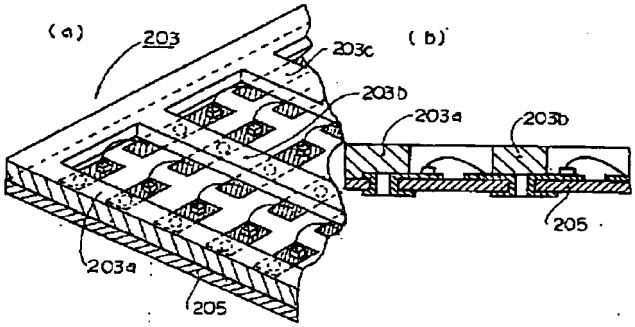
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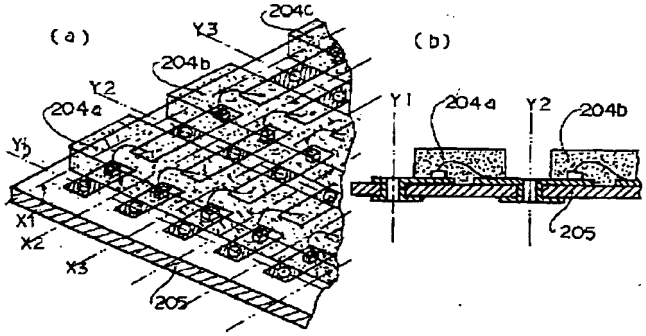
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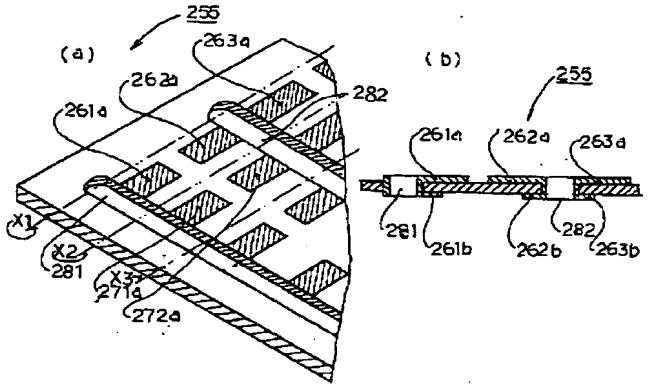
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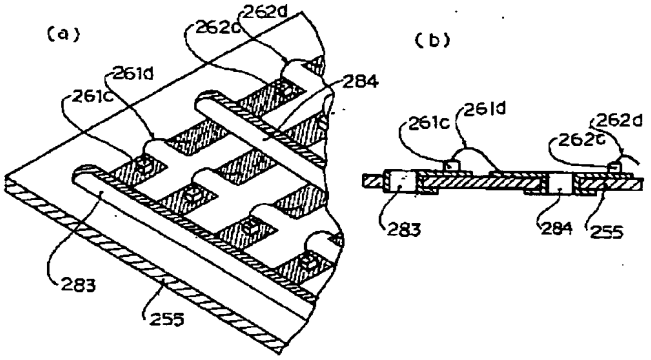
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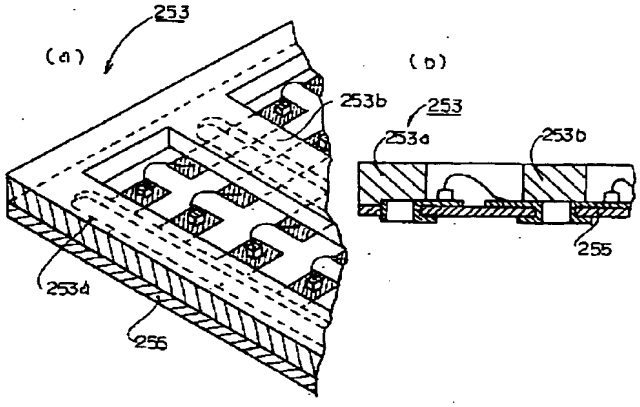
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